BE 000020

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 343 278 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 88108525.2

(22) Date of filing: 27.05.88

(51) Int. Cl.[4]: **H03H 17/02**

(43) Date of publication of application: 29.11.89 Bulletin 89/48

(84) Designated Contracting States: AT BE CH DE FR GB IT LI LU NL SE

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(54) Digital filter.

(57) While wave digital filters (WDFs) can always be implemented by commercially available integrated digital signal processors (DSPs), the efficiency of such implementations leaves room for improvement. Modified forms of WDFs are therefore derived that yield DSP implementations much more efficient than those previously available. The approach is particularly suitable for lattice WDFs. The modified WDF-structures can be easily built in such a way that they possess all stability properties desired under signal quantization, thus not only absence of small- and large-scale limit cycles but even e.g. forced-response stability and related properties.

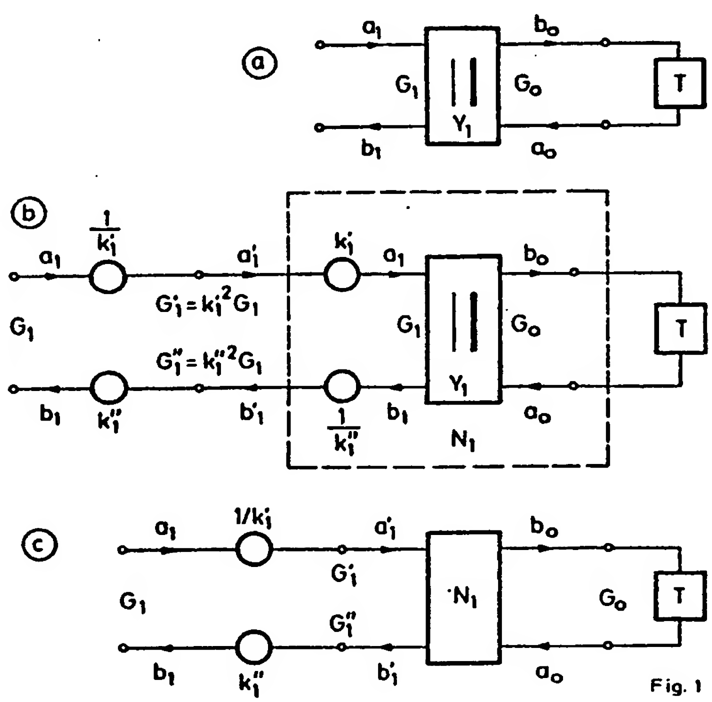

Fig. 1

EP 0 343 278 A1

Digital Filter

1. Introduction

Wave digital filters (WDFs) /1/ are known to have many interesting properties /2/. The most important of these concern their excellent stability behavior, in particular with respect to all aspects resulting from the nonlinearities that are caused by the signal quantizing operations required for carrying out rounding/truncation and overflow correction, and their good dynamic range performance. Other advantageous properties hold more specifically for voltage-wave digital filters (VWDFs), i.e., the type of WDFs usually considered and with which the present paper is also concerned: the small number of multipliers required, at least if the most appropriate structures are selected, and the small number of nonzero bits needed for implementing the multiplier coefficients.

On the other hand, VWDFs require more adders than multipliers, at least if the most common type of implementation is adopted, i.e., the one that is the most economical in number of multipliers. This is not a disadvantage if a dedicated hardware is used, but can be undesirable if the implementation should be done by means of general-purpose digital signal processors of the types hitherto available. For these digital signal processors an individual computing cycle consists indeed always of one multiplication combined with an accumulation (addition). Hence, an individual addition requires a full cycle, i.e., a multiplication by 1 followed by the addition itself. This can be a disadvantage for the implementation of WDFs, especially in the case of floating-point arithmetic. Recall that in a WDF the arithmetic operators (adders and multipliers) are grouped in so-called adaptors.

The purpose of the present method is to show how the disadvantage just mentioned can be overcome in a wide class of WDFs, i.e., those for which only two-port adaptors are neeed, by reducing appreciably the number of cycles needed for carrying out the computations. This class includes the most attractive realization of lattice WDFs, i.e. those types of WDFs that have proved so far to be the most attractive ones in practice. It will be seen that the realizations thus obtained are such that they can make use to great advantage of a feature available in several digital signal processors (see e.g. /3/). This feature allows one indeed to ensure that if an overflow occurs after a multiply-add operation the result is directly obtained according to a saturation characteristic. Due to the specific properties of WDFs this guarantees not only suppression of overflow oscillations, but also forced-response stability and related properties /2,4-8/.

Although we have so far stressed two-port adaptors, the method is also applicable in the case of adaptors with more than two ports. Considerable advantages are then still obtainable, but the reduction in number of cycles decreases with the number of ports of the adaptor. Note however that more than three ports are rarely needed in practice.

The crux of the method consists in inserting, at selected locations of the original structure, appropriately chosen pairs of inverse multipliers and then to combine each such multiplier with the adaptor to which it is adjacent. The pairs of inverse multipliers do not necessarily correspond to ideal transformers. Hence, we may no longer simply speak of port resistances or conductances (weights), but the two terminals of a same terminal-pair in the final structure may very well have different weights. This answers in a positive way a question that had been left open in a recent paper on fully general passive and lossless digital filter structures /9/. It had indeed been mentioned there that it was "not known whether there exist situations in which further simplifications could result" by choosing distinct weights for the two terminals of a same terminal-pair.

If not otherwise mentioned, terminology and notation will be as given in /2/.

2. Reactances and all-pass structures involving two-port adaptors

2.1 First-degree sections

Since WDFs are based on using wave quantities rather than voltages and currents, realizing an impedance or admittance is equivalent to realizing a reflectance; in particular realizing a reactance is equivalent to realizing an all-pass structur . A first-degree all-pass section is shown in Fig. 1a. Contrary to what we have priviously usually done /2/, we have indicated port conductances (weights) rather than port resistances, and we will do the same in corresponding later figures in this paper, such conductances (weights) being of course positive quantities. Consequently, for the multiplier coefficient γ_l we have

$\gamma_l = (G_2-G_l)/(G_l+G_2)$, $|\gamma_l| < l$, (1a,b)
and the equations describing the two-port adaptor are
$b_o = -\gamma_l a_o + (l+\gamma_l)a_l$, (2a)
$b_l = (l-\gamma_l)a_o + \gamma_l a_l$, (2b)
the subscript l being given to γ for reasons that will become clear later. We may assume $\gamma \neq 0$ since otherwise the equations (2) become trivial and a problem of simplifying them does not arise.

We now insert pairs of inverse multipliers with coefficients k_l' , l/k_l' , k_l'' , and l/k_l'' as shown in Fig. 1b. Observe that the two multipliers of such a pair are placed directly in cascade. This does not change the signals a_l and b_l at the input port of the overall arrangement. We can combine the adaptor and its two adjacent multipliers into a new building block, N_l, as indicated by means of a broken line in Fig. 1b. This building block may be said to be frequency-independent just like an adaptor since it does not contain any delay. From Fig. 1b we derive

$$a_1 = k_1' a_1' , \quad b_1 = k_1'' b_1' . \qquad (3a;b)$$

Hence, N_l is described by

$$b_o = \gamma_{oo} a_o + \gamma_{o1} a_1' , \qquad (4a)$$

$$b_1' = \gamma_{1o} a_o + \gamma_{11} a_1' \qquad (4b)$$

where

$$\gamma_{oo} = -\gamma_1 , \qquad \gamma_{o1} = (1+\gamma_1)k_1' . \qquad (5a,b)$$

$$\gamma_{1o} = (1-\gamma_1)/k_1'' , \qquad \gamma_{11} = \gamma_1 k_1'/k_1'' . \qquad (5c,d)$$

We have two alternatives for making equal to unity one of the coefficients in each one of the equations (4a) and (4b). The first alternative is

$$k_1' = 1/(1+\gamma_1) , \quad k_1'' = 1-\gamma_1 . \quad k_1''/k_1' = 1-\gamma_1^2 , \qquad (6a,b,c)$$

which leads to
$\gamma_{oo} = -\gamma_l$, $\gamma_{ol} = \gamma_{lo} = l$, $\gamma_{ll} = \gamma_l/(l-\gamma_l^2)$. (7)
The second alternative is

$$k_1' = 1/(1+\gamma_1) , \quad k_1'' = \gamma_1/(1+\gamma_1) , \quad k_1''/k_1' = \gamma_1 \qquad (8a,b,c)$$

and leads to
$\gamma_{oo} = -\gamma_l$, $\gamma_{ol} = \gamma_{ll} = l$, $\gamma_{lo} = (l-\gamma_l^2)/\gamma_l$. (9)
Since $|\gamma_l| < l$, we can always ensure, if desired, that none of the coefficients in (4) is larger than l in modulus. This possibility is offered by (6) and (7) for $|\gamma_l| \leq (\sqrt{5}-l)/2 \approx 0{,}618$, and by (8) and (9) for $|\gamma_l| \geq (\sqrt{5}-l)/2$. In (6) and (8) we have supplemented the expressions for k_l' and k_l'' simple expressions for k_l''/k_l' ; these show that we always have

$$|k_1''/k_1'| \leq 1 \ . \qquad (10)$$

There remain of course the two multipliers to the left of N_l in Figs. 1b and 1c. These may obviously be combined into a single multiplier of coefficient k_l''/k_l'. In some cases this signle multiplier may even simply be dropped, but in others, this is not permitted. In any case, the implementation of N_l requires only 2 multiply-accumulate steps. A simplified overall representation of the structure of Fig. 1b is shown in Fig. 1c.

In addition to the port conductances G_o and G_l, the weights

$$G_1' = k_1'^2 G_1 \ , \qquad G_1'' = k_1''^2 G_1 \ , \qquad (11a,b)$$

are indicated in Fig. 1b and 1c. Only G_o corresponds to a true port conductance, while G_l' and G_l'' are the individual terminal weights of the two terminals of N_l at its access on the left. These two terminals thus do not form a true port. The role played by G_l' and G_l'' will become clear in Section 3.

It is obvious from what we have said that N_l may be no longer termed a two-port, although it is a four-terminal (building) block or, simpler, a 4-pole block.

2.2 Sections of degree two and higher

A situation in which the multipliers to the left of N_l mentioned in Subsection 2.1 may not immediately be dropped is encountered in a second-degree all-pass section as shown in Fig. 2a. Note that we could there combine the two delays T/2 into a single delay T, but we have preferred keeping them separate for the sake of symmetry and for reasons as explained in /2/. We can again transform Fig. 2a in a way similar to what we have done previously, which leads to Fig. 2b. The port to the right in Fig. 2a is assumed to be transformed as in Fig. 1, with N_l thus being as in Figs. 1b and 1c. The multipliers l/k_l' and k_l'', however, have been shifted across the two delays T/2 and have been inserted into what is becoming N_2. In addition to the weights G_l', and G_l'' given by (10) we now also have to consider terminal weights

$$G_2' = k_2'^2 G_2 \ , \qquad G_2'' = k_2''^2 G_2 \ . \qquad (12)$$

A simplified overall representation of the structure of Fig. 2b is shown in Fig. 2c.

The equations describing the left adaptor in Fig. 2a are

$$b_2 = -\gamma_2 a_2 + (1+\gamma_2) a_3 \ , \qquad (13a)$$

$$b_3 = (1-\gamma_2) a_2 + \gamma_2 a_3 \ , \qquad (13b)$$

where

$\gamma_2 = (G_2-G_l)/(G_2+G_l)$, $|\gamma_2| < l$, (14a,b)

(14b) following again from (14a) because $G_l>0$ and $G_2>0$. We may assume $\gamma_2 \neq 0$. Since (cf. Fig. 2b)

$$a_2 = k_1'' a_2' \ , \qquad b_2 = k_1' b_2' \ , \qquad (15a,b)$$

$$a_3 = k_2' a_3' \qquad b_3 = k_2'' b_3' \ , \qquad (15c,d)$$

(13) gives rise to

$$b_2' = \gamma_{22} a_2' + \gamma_{23} a_3' , \tag{16a}$$

$$b_3' = \gamma_{32} a_2' + \gamma_{33} a_3' \tag{16b}$$

where

$$\gamma_{22} = -\gamma_2 k_1''/k_1' , \qquad \gamma_{23} = (1+\gamma_2) k_2'/k_1' , \tag{17a,b}$$

$$\gamma_{32} = (1-\gamma_2) k_1''/k_2'' , \qquad \gamma_{33} = \gamma_2 k_2'/k_2'' . \tag{17c,d}$$

These equations thus describe a new 4-pole block, N_2, indicated in Fig. 2b by means of a broken line and shown in compact form in Fig. 2c.

In (15), k_2', and k_2'' may be chosen arbitrarily, but γ_{22} cannot be influenced by the choice available. Like for N_1, we have thus two choices for making equal to unity one of the coefficients in each one of the equations (16a) and (16b), i.e., on the one hand,

$$k_2' = k_1'/(1+\gamma_2) , \quad k_2'' = (1-\gamma_2) k_1'' , \tag{18a,b}$$

which leads to

$$\gamma_{22} = -\gamma_2 k_1''/k_1' , \quad \gamma_{23} = 1 \tag{19a,b}$$

$$\gamma_{32} = 1 , \quad \gamma_{33} = \frac{\gamma_2}{1-\gamma_2^2} \cdot \frac{k_1'}{k_1''} , \tag{19c,d}$$

and on the other,

$$k_2' = k_1'/(1+\gamma_2) , \quad k_2'' = \gamma_2 k_2' , \tag{20a,b}$$

which leads to

$$\gamma_{22} = -\gamma_2 k_2''/k_1' , \quad \gamma_{23} = 1 , \tag{21a,b}$$

$$\gamma_{32} = \frac{1-\gamma_2^2}{\gamma_2} \cdot \frac{k_1''}{k_1'} , \quad \gamma_{33} = 1 . \tag{21c,d}$$

These two choices still have to be combined with those available for N_1, i.e., for k_1' and k_1'', thus yielding altogether four choices. Due to $|\gamma_2| < 1$, taking into account (10), we can always ensure that none of the coefficients in (16) is larger than unity in modulus, and this independently of which one of the alternatives

for N_t has been adopted. The property mentioned is indeed achieved by (19) or (21) if

$$|\gamma_2/(1-\gamma_2^2)| \leq |k_1''/k_1'| \text{ or } |\gamma_2/(1-\gamma_2^2)| \geq |k_1''/k_1'| , \quad (22)$$

respectively. Note that from (18) and (20b) we also obtain

$$k_2''/k_2' = (1-\gamma_2^2)k_1''/k_1' \quad \text{and} \quad k_2''/k_2' = \gamma_2 , \quad (23)$$

respectively. These expressions together with (10) show that we have in all cases

$$|k_2''/k_2'| \leq 1 . \quad (24)$$

The process described can be obviously extended to all-pass structures of arbitrary degree, say n (Fig. 3a). We then proceed from the right to the left as we have done in Fig. 2, and we thus arrive at a structure of the form given in Fig. 3b. The derivation of N_3 will be exactly as that of N_2, but with k_2' and k_2'' taking the role of k_1' and k_1'' etc. The equations describing the i-th two-port parallel adaptor, i=l to n, are given by

$$b_{2i-2} = -\gamma_i a_{2i-2} + (1+\gamma_i)a_{2i-1} , \quad (25a)$$

$$b_{2i-1} = (1-\gamma_i)a_{2i-2} + \gamma_i a_{2i-1} , \quad (25b)$$

where

$\gamma_i = (G_i-G_{i-1})/(G_i+G_{i-1})$ $|\gamma_i| < 1$, (26a,b)

the G_o to G_n being the consecutive port conductances. We introduce parameters k_1' to k_n' and k_1'' to k_n'' as well as new signal quantities a_o' to a'_{2n-1} and b_o' to b'_{2n-1} satisfying, for i=l to n, the equations

$$a_{2i-2} = k''_{i-1}a'_{2i-2} , \quad b_{2i-2} = k'_{i-1}b'_{2i-2} , \quad (27a,b)$$

$$a_{2i-1} = k'_i a'_{2i-1} , \quad b_{2i-1} = k''_i b'_{2i-1} , \quad (27c,d)$$

with

$$k_o' = k_o'' = 1 , \; a_o' = a_o , \; b_o' = b_o . \quad (28a,b,c,d)$$

This leads to

$$b'_{2i-2} = \gamma_{2i-2,2i-2}\, a'_{2i-2} + \gamma_{2i-2,2i-1}a'_{2i-1} , \quad (29a)$$

$$b'_{2i-1} = \gamma_{2i-1,2i-2}\, a'_{2i-2} + \gamma_{2i-1,2i-1}a'_{2i-1} , \quad (29b)$$

where

$$\gamma_{2i-2,2i-2} = -\gamma_i \frac{k''_{i-1}}{k'_{i-1}} , \quad \gamma_{2i-2,2i-1} = (1+\gamma_i) \frac{k'_i}{k'_{i-1}} , \quad (30a,b)$$

$$\gamma_{2i-1,2i-2} = (1-\gamma_i) \frac{k''_{i-1}}{k''_i} , \quad \gamma_{2i-1,2i-1} = \gamma_i \frac{k'_i}{k''_i} . \quad (30c,d)$$

These equations thus describe the 4-pole block N_i. For the terminal weights of N_i one finds

$$G'_i = k'^2_i G_i , \quad G''_i = k''^2_i G_i , \quad (31)$$

at least for those at the left-hand side of N_i. At the right-hand side of N_i the terminal weights are the sam as the corresponding ones at the left-hand side of N_{i-1}. They are thus those given by (31), but with i replaced by i-l. In view of (28a,b) this includes the case i=l.

By appropriate choice of the k'_i and k''_i, we can make sure that, for each i=l to n, one of the coefficients in (29a) and one of the coefficients in (29b) becomes equal to unity. Each one of the N_i, i=l to n, thus requires only two multiply-accumulate steps. The two solutions for which this holds are

$$k'_i = k'_{i-1}/(1+\gamma_i) , \quad k''_i = (1-\gamma_i)k''_{i-1}) \quad (32a,b)$$

which leads to

$$\gamma_{2i-2,2i-2} = -\gamma_i k''_{i-1}/k'_{i-1}, \quad \gamma_{2i-2,2i-1} = 1 , \quad (33a,b)$$

$$\gamma_{2i-1,2i-2} = 1 , \quad \gamma_{2i-1,2i-1} = \frac{\gamma_i}{1-\gamma_i^2} \cdot \frac{k'_{i-1}}{k'_{i-1}} , \quad (33c,d)$$

and

$$k'_i = k'_{i-1}/(1+\gamma_i) , \quad k''_i = k'_{i-1}\gamma_i/(1+\gamma_i) , \quad (34a,b)$$

which leads to

$$\gamma_{2i-2,2i-2} = -\gamma_i k''_{i-1}/k'_{i-1}, \quad \gamma_{2i-2,2i-1} = 1 , \quad (35a,b)$$

$$\gamma_{2i-1,2i-2} = \frac{1-\gamma_i^2}{\gamma_i} \cdot \frac{k''_{i-1}}{k'_{i-1}} , \quad \gamma_{2i-1,2i-1} = 1 . \quad (35c,d)$$

Furthermore, one of the two alternatives thus available for N_i is such that it does not imply any

multiplier coefficient larger than l in modulus. Mor precisely, whil we have in general 2^n possibilities for achieving the goal that none of the N_l to N_n requires more than two multiply-accumulate steps, there is always one solution, and usually also only one, for which none of the final multiplier coefficients is larger than one in modulus. This can be shown to be a consequence, among other things, of the fact that one has always either

$$\frac{k_i''}{k_i'} = (1-\gamma_i^2)\frac{k_{i-1}''}{k_{i-1}'} \quad \text{or} \quad \frac{k_i''}{k_i'} = \gamma_i ,$$

thus, in view of (26b) and (28a,b),

$$|k_i''/k_i'| \leq 1 \quad \text{for} \quad i = 1 \text{ to } n. \qquad (36)$$

This is also the reason why it is never possible to arrive at a choice such as $\gamma_{2i-2,2i-2} = 1$.

The two multipliers remaining at the left of Fig. 3b can be combined into a single multiplier $m = k_n''/k_n'$, for which we thus also have $|m| \leq 1$, with the inequality sign usually holding. In some cases this single multiplier may even simply be dropped, in others, it may in turn be combined in some fashion with another multiplier, thus leading also to a further saving.

We conclude this section by listing a few useful relations that can be derived after some more or less tedious calculations. For the solution defined by (32) and (33) we obtain, using (26) and (31),

$$\gamma_{2i-2,2i-2}^2 - \frac{\gamma_{2i-2,2i-2}}{\gamma_{2i-1,2i-1}} = \frac{G_{i-1}''}{G_{i-1}'} \qquad (37)$$

$$\frac{G_i'}{G_{i-1}''} = -\frac{\gamma_{2i-1,2i-1}}{\gamma_{2i-2,2i-2}} , \quad \frac{G_i''}{G_{i-1}'} = -\frac{\gamma_{2i-2,2i-2}}{\gamma_{2i-1,2i-1}} \qquad (38a,b)$$

$$G_i'G_i'' = G_{i-1}'G_{i-1}'' , \quad G_i' = (1-\gamma_{2i-2,2i-2}\,\gamma_{2i-1,2i-1})G_{i-1}' . \qquad (39a,b)$$

Similarly, for the solution defined by (34) and (35) we obtain, using again (26) and (31),

$$\gamma_{2i-2,2i-2}^2 - \gamma_{2i-2,2i-2}\,\gamma_{2i-1,2i-2} = \frac{G_{i-1}''}{G_{i-1}'} , \qquad (40)$$

$$\frac{G_i'}{G_{i-1}''} = -\frac{1}{\gamma_{2i-2,2i-2}\cdot\gamma_{2i-1,2i-2}} , \quad \frac{G_i''}{G_{i-1}'} = -\frac{\gamma_{2i-2,2i-2}}{\gamma_{2i-1,2i-2}} , \qquad (41a,b)$$

$$G_i' = G_{i-1}' + G_i'' , \quad G_i' = \left(1 - \frac{\gamma_{2i-2,2i-2}}{\gamma_{2i-1,2i-2}}\right) G_{i-1}' . \qquad (42,a,b)$$

<u>3. Realization of circuits with more than 2 terminals</u>

WDFs in lattice configuration hav so far turned out to be th most attractive ones from a practical point of view /2/. A lattice WDF can be built by means of two WDF all-pass structures. For these, the results of Section 2 are immediately applicable. In fact, one can make use of these results in different fashions since any all-pass function can be realized by means either of a chain connection of unit elements or a cascade of individual sections of degree, say, one and two. In the former case, we obtain a WDF realization in the form of Fig. 3a, thus leading to the structure of Fig. 3b. In the latter, we are lead to making use of th results described in relation with Figs. 1 and 2. In all cases, however, there obviously will be, for each complete all-pass structure, only one multiplier that has to be implemented in addition to those inside of building blocks such as N_l to N_n in Figs. 1 to 3, i.e., in addition to those implemented in form of mulipIy-accumulate operations.

A configuration of a lattice WDF for the case that only one input and one output terminal is used is shown in Fig. 4a. It comprises two branches of all-pass transfer functions S_l and S_2, while A_l and B_2 are th (steady-state or z-transform) input and output signals, respectively. (The factor 2 at the output is irrelevant; it has been included in order to be in conformity with Fig. 23 in /2/.) Let S_l' and S_2' be those functions corresponding to S_l and S_2, respectively, that are obtained by the method explained in Section 2 if we ignore the remaining multipliers mentioned in the previous paragraph.

Clearly, the structure of Fig. 4a is equivalent to that of Fig. 4b where m_l and m_2 are the coefficients of the multipliers just referred to. Clearly, the structure of Fig. 4b is equivalent to those of Fig. 4c and 4d. In these, the multipliers m_l and m_2, respectively, may again usually be dropped, and the remaining multiplier may be combined with the adder into another multiply-accumulate operation. Note that the discussion given here does not consider scaling requirements.

The situation is, obviously, very similar if the full two-port lattice WDF (Fig. 5a) is to be implemented. One of the two main possibilities then available is shown in Fig. 5b.

There are also other WDF structures for which the method is directly applicable. This is the case in particular for a WDF (Fig. 6b) obtained from a reference filter in form of a cascade of unit elements (Fig. 6a). We may in this case again start from the end with the port conductance G_o, similar to what we have done in Section 2, and then proceed to the other end, which leads us to the structure of Fig. 6c. Note that in Fig. 6 we have adopted a numbering of the G_i, $i=0$ to $n+l$, which is different from the one we have usually chosen in the case of doubly-terminated filters /2/, but which is more in conformity with the on used in Figs. 1 to 3.

The process is precisely as that described in Section 2, except at the beginning. Indeed, assuming that a multiplier in cascade with an externally accessible terminal is irrelevant, we may introduce multipliers l/k_o'' and k_o' in cascade with the input and the output terminal, respectively, of port 0. If we choose $k_o' = k_o'' = l$ (cf. (28a,b)) everything will be as in Section 2, but if we accept $k_o' \neq k_o''$ we have one additional degree of freedom. This may be used to make one further coefficient (e.g. in N_l) equal to unity.

The methods explained in this section may, of course, also be of interest in the case of circuits having more than one input and more than one output terminal.

4. Stability considerations

4.1 Ideal lossless building blocks

It is known that the most important advantages of WDFs are their excellent stability properties, especially those under the various nonlinear conditions resulting from the unavoidable quantization operations needed for the signal quantities. Due to the way we have derived the new circuits described in Sections 2 and 3, from conventional WDFs it follows that the former must inherit all stability properties of the latter. We will briefly examine the mechanism behind this observation. We do this first under th assumption of ideal lossless building blocks N_i. The case of nonideal blocks N_i will be considered in Subsection 4.2.

Consider thus a 4-pole N_i, $i \in \{1,2,\ldots,n\}$, of Fig. 3. It is described by the equations (26) to (31), the latter to be used, for a given N_i, also with i replaced by i-l. In order to simplify the writing, we consider specifically the case $i=2$, in which case the equations just mentioned may be replaced by (11), (12), and (14) to (17). (Note that $i=l$ would not be appropriate if one wants to be general, since for N_l the specific conditions (28) hold.)

The instantaneous power (pseudopower) absorbed by the original adaptor with coefficient γ_2 is given by

$$p_2 = (G_l a_2^2 + G_2 a_3^2) - (G_l b_2^2 + G_2 b_3^2) \qquad (43)$$

It is known (and can be verified directly) that, due to losslessness, we have $p_2 = 0$. Using (11), (12), and (15), we obtain from (43),

$$p_2 = (G_1'' a_2'^2 + G_2' a_3'^2) - (G_1' b_2'^2 + G_2'' b_3'^2) . \qquad (44)$$

We note that in (44) each one of the four signals a_2', a_3', b_2', and b_3' appears squared and multiplied by the weight of the particular terminal to which the signal refers. Under ideal linear conditions, i.e., if (16) holds, (44) yields again $p_2 = 0$, assuming of course that (11), (12), (14a), and (17) are satisfied.

Mathematically speaking, the main difference between (43) and (44) consists in the fact that while in (43) the second paranthesis comprises the same weights (i.e., G_1 and G_2) as the first one, this is not the case for (44). It is known however /2,9,10/ that this does not affect any of the stability proofs that have been provided for WDFs. This implies that the same type of quantization rules that guarantee, if applied to the b_i, a specific type of stability in the original WDF, will guarantee the same type of stability in the modified WDF if applied to the b_i', with i ranging over an appropriate set of integers.

In order to be more specific, let us designate by b_{iq}' the value resulting from b_i' by quantization. There will be no observable small-scale or large-scale limit cycle if quantization is carried out in such a way that $|b_{iq}'| \leq |b_i'|$ for all relevant values of i. If the circuit is such that it cannot sustain unobservable periodic oscillations under ideal linear conditions and if the rule adopted for overflow corrections is such that a simple sign inversion is excluded, there will be no unobservable limit cycle either. The conditions mentioned allow us also to guarantee stability under looped conditions and to state equally that the limit cycles superposed to the output signal if the input is an arbitrary periodic signal will be very small.

Of particular interest finally is the fact that forced-response stability and related properties /4-8/ can be guaranteed by simply requiring that for all relevant i's the value of b_{iq}' is obtained from the corresponding b_i' by adopting for overflow correction e.g. either simple saturation or a triangular overflow characteristic with slopes of ±45°. The first of these possibilities is directly available in several digital signal processor (e.g. in the TMS 320 /3/) at the completion of each multiply-accumulate step. Thus, since the computation of any b_{iq}' requires just one such step, using the option available in such a digital signal processor automatically guarantees forced-response stability and related properties.

It should be stressed that all this holds for any type of signal representation, in particular thus not only for fixed-point arithmetic but also for floating-point arithmetic. This is particularly important since any floating-point digital filter that cannot be built strictly without parasitic oscillation can always sustain a parasitic oscillation involving the highest possible value of the exponent /11,12/, in practice thus a parasitic oscillation of high amplitude.

It should finally be recalled that an expression such as that appearing in the right-hand side of (44) corresponds indeed to the definition of the power absorbed in the case of a class of digital filters that appears to be the only one that offers all the same good features as conventional WDFs, yet is in a sense somewhat more general /9/. It had been shown in /9/ that this extended class can always be obtained from conventional WDFs by precisely the type of transformation described in Section 2. Since this type of transformation is of rahter trivial nature, the digital filters described in this paper should still appropriately be called "wave digital filters".

In /9/ the question had been left open whether the transformation just referred to can lead to structures offering true advantages over those obtainable by the more conventional WDF approach. The results of the present paper show that this question can now be answered in the affirmative.

4.2 Lossy building blocks

In a conventional WDF an adaptor can be easily made strictly lossless, at least under the assumption that all additions and multiplications are carried out exactlxy, i.e., that the circuit is strictly linear. This is due to the fact that e.g. for a two-port adaptor described by (13) strict losslessness is fulfilled for any value of γ_2 provided we adopt port weights G_1 and G_2 that satisfy (14). Since the latter requirement is trivial to meet, we can, in particular, adopt for γ_2 any value expressible in a binary representation with finite number of bits. In this case, all four coefficients in (13), in particular thus also the coefficients $(1-\gamma_2)$ and $(1+\gamma_2)$, are expressible in the ssam way.

This same simple property does not hold for the blocks N_i, i = l to n, say, in an all-pass section of the type of Fig. 3b. In order to show this we simply consider N_1. Since $G_0' = G_0'' = G_0$ we obtain, for i = l, from

(37) and (40)

$$\gamma_{oo}^2 - \frac{\gamma_{oo}}{\gamma_{11}} = 1 \quad \text{and} \quad \gamma_{oo}^2 - \gamma_{oo}\gamma_{1o} = 1 \ , \qquad (45a,b)$$

respectively. Thus γ_{oo} and γ_{ll} (first equation) as well as γ_{oo} and γ_{lo} (second equation) have to satisfy an expression that usually cannot be fulfilled if these coefficients have to be expressed in a finite number of binary digits.

In order to solve this dilemma we observe that for all stability aspects discussed in Subsection 4.1 to hold it is merely required that the blocks N_l are passive, i.e., such that $p_i \geq 0$, $i = l$ to n, and this for all values of the input signals of N_l, p_i being defined as given by (44) (for $i = 2$); strict losslessness, i.e., $p_i = 0$ instead of $p_i \geq 0$, is not needed.

We first consider N_l, more specifically the choice leading to (7). Let γ_{ooq} and γ_{llq} be the quantized values of γ_{oo} and γ_{ll}, respectively. We may assume the value of G_o to be given, but G_l' and G may have to be replaced by new values, which we designate by G'_{lq} and G''_{lq}, respectively; suitable choices for these still have to determined. Let p_{lq} be the power absorbed by N_l under these new conditions. We have

$$p_{1q} = G_o a_o^2 + G'_{1q} a_1'^2 - G_o b_o^2 - G''_{1q} b_1'^2 \ . \qquad (46)$$

Using (4) (but with γ_{oo} and γ_{ll} replaced by γ_{ooq} and γ_{llq}, respectively) and $\gamma_{ol} = \gamma_{lo} = l$, this yields

$$p_{1q} = (G_o - \gamma_{ooq}^2 G_o - G''_{1q}) a_o^2 + (G'_{1q} - G_o - \gamma_{11q}^2 G''_{1q}) a_1'^2$$
$$- 2(\gamma_{ooq} G_o + \gamma_{11q} G''_{1q}) a_o a_1' \ . \qquad (47)$$

Any choice of γ_{ooq}, γ_{llq}, G'_{lq}, and G''_{lq} for which $p_{lq} \geq 0$ for all a_o and a_l' is acceptable.

We will now show that the problem thus formulated is indeed solvable. For this, let us choose G'_{lq} and G''_{lq} such that

$$G'_{1q} = (1 - \gamma_{ooq}\gamma_{11q}) G_o \ , \qquad G''_{1q} = -\frac{\gamma_{ooq}}{\gamma_{11q}} G_o \ , \qquad (48a,b)$$

these expressions corresponding in a sense to (39b) and (38b), respectively, with $i = l$. In order to lead to the desired stability results, these expressions must yield positive values of the weights G'_{lq} and G''_{lq}. For this, observe that in view of (1b) and (7) we have $\gamma_{oo}\gamma_{ll} < 0$, and we may thus assume the quantization to be such that the signs of γ_{oo} and γ_{ll} are not reversed, i.e., in particular, that
$-\gamma_{ooq}\,\gamma_{llq} \geq 0$, $-\gamma_{ooq}/\gamma_{llq} \geq 0$. (49) Substitution of (48) in (47) yields

$$p_{1q} = \left(1 - \gamma_{ooq}^2 + \frac{\gamma_{ooq}}{\gamma_{11q}}\right) G_o a_o^2 \qquad (50)$$

and thus requires
$\gamma_{ooq}^2 - (\gamma_{ooq}/\gamma_{llq}) \leq l$. (51)
which, in view of (49), is equivalent to
$\gamma_{ooq}^2 + |\gamma_{ooq}/\gamma_{llq}| \leq l$. (52)

Comparison with (45a) shows that it is easy to carry out a quantization of γ_{oo} and γ_{ll} such that (51) is fulfilled. All requirements are then m t if G'_{lq} and G''_{lq} are chosen according to (48).

Next we consider again N_l, but with the choice leading to (9). From (46) we now obtain

$$p_{1q} = (G_o - \gamma_{ooq}^2 G_o - \gamma_{1oq}^2 G''_{1q}) a_o^2 + (G'_{1q} - G_o - G''_{1q}) a_1'^2$$

$$- 2(\gamma_{ooq} G_o + \gamma_{1oq} G''_{1q}) a_o a_1' . \qquad (53)$$

By an approach similar to that used before one finds that $p_{lq} \geq 0$ for all a_o and a_l' if e.g. we quantize γ_{oo} and γ_{lo} in such a way that
$\gamma^2_{ooq} - \gamma_{ooq}\gamma_{loq} \leq l$, (54)
and if we select G'_{lq} and G''_{lq} such that (cf. (41b) and (42a) for i = l)

$$G''_{1q} = -(\gamma_{ooq}/\gamma_{1oq}) G_o ; \qquad G'_{1q} = G''_{1q} + G_o \quad . \qquad (55a,b)$$

Assume next that the circuit involves also N_2. Having performed a quantization of the coefficients of N_l and having thus also chosen G'_{lq} and G''_{lq}, we may now approach N_2. We assume first that for N_2 the choice leading to (19) has been adopted. Let γ_{22q} and γ_{33q} be the quantized versions of γ_{22} and γ_{33}, respectively, let G'_{2q} and G''_{2q} be corresponding choices for G_2' and G_2'', respectively, and let p_{2q} be the value thus replacing p_2 given by (44). We have

$$p_{2q} = G''_{1q} a_2'^2 + G'_{2q} a_3'^2 - G'_{1q} b_2'^2 - G''_{2q} b_3'^2 \quad . \qquad (56)$$

From this we obtain, using (16) (with γ_{22} and γ_{33} replaced by γ_{22q} and γ_{33q}, respectively) together with (19b) and (19c),

$$p_{2q} = (G''_{1q} - \gamma_{22q}^2 G'_{1q} - G''_{2q}) a_2'^2 + (G'_{2q} - G'_{1q} - \gamma_{33q}^2 G''_{2q}) a_3'^2$$

$$- 2(\gamma_{22q} G'_{1q} + \gamma_{33q} G''_{2q}) a_2' a_3' \quad , \qquad (57)$$

where G'_{lq} and G''_{lq} may be assumed to be known from quantizing the coefficients of N_l. Any choice of γ_{22q}, γ_{33q}, G'_{2q}, and G''_{2q} for which $p_{2q} \geq 0$ for all a_2' and a_3' is acceptable.

One such choice is obtained if we put

$$G'_{2q} = (1 - \gamma_{22q}\gamma_{33q}) G'_{1q} \quad , \qquad G''_{2q} = -(\gamma_{22q}/\gamma_{33q}) G'_{1q} \quad , \qquad (58a,b)$$

these expressions corresponding in a sense to (39b) and (38b), respectively, with i = 2. This leads again to positive weights G'_{2q} and G''_{2q}; indeed it follows from (14b), (19a), and (19d) that $\gamma_{22}\gamma_{33} < 0$ so that we may assume
$\gamma_{22q}\ \gamma_{33q} < 0$, $\gamma_{22q}/\gamma_{33q} < 0$. (59)
Inserting (58) into (57) leads to

$$p_{2q} = (G''_{1q} - \gamma_{22q}^2 G'_{1q} + (\gamma_{22q}/\gamma_{33q}) G'_{1q}) a_2'^2 \quad , \qquad (60)$$

from which we derive the requirement

$$\gamma_{22q}^2 - (\gamma_{22q}/\gamma_{33q}) \leq G''_{1q}/G'_{1q} \ . \qquad (61)$$

Hence, a quantization according to (61) together with a choice of G'_{2q} and G''_{2q} according to (58) meets all the requirements.

If for N_2 we adopt the choice leading to (21), it turns out that (57) is replaced by

$$p_{2q} = (G''_{1q} - \gamma_{22q}^2 G'_{1q} - \gamma_{32q}^2 G''_{2q})a_2'^2 + (G'_{2q} - G'_{1q}\ G''_{2q})a_3'^2$$

$$- 2(\gamma_{22q}G'_{1q} + \gamma_{32q}G''_{2q})a_2'a_3' \ . \qquad (62)$$

We now have to perform the quantization of γ_{22} and γ_{32} as well as the choice of G'_{2q} and G''_{2q} in such a way that $p_{2q} \geq 0$ for all a_2' and a_3' . A possible simple solution for this can be found in a similar way as before, i.e., by combining the requirement

$$\gamma_{22q}^2 - \gamma_{22q}\ \gamma_{32q} \leq G''_{1q}/G'_{1q} \qquad (63)$$

with the choice

$$G''_{2q} = -(\gamma_{22q}/\gamma_{32q})G'_{1q} \qquad G'_{2q} = G'_{1q} + G''_{2q} \ . \qquad (64a,b)$$

If $n > 2$, the process can be continued until we reach N_n. Thus, for any $i \in \{1,2,\ldots,n\}$ and with $G'_{i-1,q}$ and $G''_{i-1,q}$ known, we must quantize the coefficients of N_i in such a way that $p_{iq} \geq 0$ for all choices of a'_{2i-1} and a'_{2i-2}, with

$$p_{iq} = G''_{i-1,q}a'^2_{2i-2} + G'_{iq}a'^2_{2i-1} - G'_{i-1,q}b'^2_{2i-2} - G''_{iq}b'^2_{2i-1} \ .$$

A possible solution for this is immediately obtained as generalization of our results given above. Thus, if for N_i we adopt the choice leading to (33) we may first quantize $\gamma_{2i-2,2i-2}$ and $\gamma_{2i-1,2i-1}$ according to

$$\gamma_{2i-2,2i-2,q}^2 - \frac{\gamma_{2i-2,2i-2,q}}{\gamma_{2i-1,2i-1,q}} \leq \frac{G''_{i-1,q}}{G'_{i-1,q}} \qquad (65)$$

and then choose G'_{iq} and G''_{iq} according to

$$G'_{iq} = (1-\gamma_{2i-2,2i-2,q}\gamma_{2i-1,2i-1,q})G'_{i-1,q} \ , \qquad (66a)$$

$$G''_{iq} = -(\gamma_{2i-2,2i-2,q}/\gamma_{2i-1,2i-1,q})G'_{i-1,q} \ . \qquad (66b)$$

Similarly, if for N_i we adopt the choice leading to (35) we may quantize $\gamma_{2i-2,2i-2}$ and $\gamma_{2i-1,2i-2}$ according to

$$\gamma^2_{2i-2,2i-2,q} - \gamma_{2i-2,2i-2,q}\gamma_{2i-1,2i-2,q} \leq \frac{G''_{i-1,q}}{G'_{i-1,q}} \qquad (67)$$

and then choose G'_{iq} and G''_{iq} according to

$$G''_{iq} = -(\gamma_{2i-2,2i-2,q}/\gamma_{2i-1,2i-2,q})G'_{i-1,q}\ , \qquad (68a)$$

$$G'_{iq} = G'_{i-1,q} + G''_{iq}\ . \qquad (68b)$$

If in such a process an optimum solution (say, with respect to the transmission properties of the circuit) is desired for the quantized coefficients, one should of course repeat the full cycle from I to n as often as needed. Note that we could then encounter, for one or more of the $i \in \{1,2,...,n\}$, a case for which one of the two multiplier coefficients may be chosen equal to zero. We then also choose the other coefficient equal to zero and we restrict this situation to the case leading to (33), thus to
$\gamma_{2i-2,2i-2,q} = \gamma_{2i-1,2i-1,q} = 0$
and

$$G'_{iq} = G'_{i-1,q}\ , \quad G''_{iq} = G''_{i-1,q}\ .$$

The problem of determing N_i thus then becomes trivial.

After having completed the quantization of the coefficients of the blocks N_i, i = I to n, there may remain the problem of choosing I/k'_n and k''_n (cf. Fig. 3b), or simply that of choosing

$$m = k''_n/k'_n\ .$$

A need for this does not arise if m may simply be dropped. In other cases such as in Fig. 4c the actual problem is that of finding a quantized value for m_2/m_1, where m_1 and m_2 in turn may be products of factors such as m, but this is not a question of stability.

There may be cases however where passivity from input to output must be guaranteed. In such cases it is best to consider the corresponding transfer function. Let thus A'_{2n-1} and B'_{2n-1} be the steady-state (or z-transform) quantities corresponding to a'_{2n-1} and b'_{2n-1}, respectively (Fig. 3b). If all blocks N_1 to N_n are designed as discussed above, i.e., if these are all passive, we have /9,10/

$$G'_n|A'_{2n-1}|^2 - G''_n|B'_{2n-1}|^2 \geq 0\ ,$$

i.e., for the transfer function S,

$$|S|^2 \leq |G'_n/G''_n| \quad \text{where} \quad S = B'_{2n-1}/A'_{2n-1}\ .$$

Note that in our stability analysis we have specifically examined the cas of the structures of Figs. 1 to

3. It is obvious that similar considerations hold for other structures, e.g. for the one of Fig. 6.

In the above procedure of quantizing the multipli r coefficients in such a way that the blocks N_i, i-l to n, remain passive, we have, for each case considered, given a specific solution by which the desired goal can be achi ved. It should be str ssed that other solutions may very well be feasible. Thus, considering the general case of N_i, adopting the choice leading to (33), we may replace (66a) by

$$G'_{iq} = -(\gamma_{2i-1,2i-1,q}/\gamma_{2i-2,2i-2,q})G''_{i-1,q} \quad . \qquad (69)$$

It can be shown indeed that performing the quantization according to (65) and selecting G $_{iq}$ and G $_{iq}$ according to (69) and (66b), respectively, also meets all the requirements.

However, such an alternative cannot be better than the one given by (65) and (66). Indeed, using (65) with i replaced by i+l, we see that the quantity $K_i = G''_{iq}/G'_{iq}$ should be as large as possible in order to facilitate as much as possible the quantization of N_{i+1}. One verifies that the ratio of the values of K_i obtained by choosing G'_{iq} according to (69) and (66a), respectively, is equal to

$$\left(\gamma^2_{2i-2,2i-2,q} - \frac{\gamma_{2i-2.2i-2,q}}{\gamma_{2i-1,2i-1,q}}\right)\frac{G'_{i-1.q}}{G''_{i-1,q}} \quad ,$$

which according to (65) is ≤l.

The situation is similar if for N_i the choice leading to (35) is considered. An alternative solution is then obtained if we replace (68b) by

$$G'_{iq} = -G''_{i-1,q}/(\gamma_{2i-2,2i-2,q}\gamma_{2i-1,2i-2,q}) \quad , \qquad (70)$$

but again, it is never better than the one given originally. The reason for this is the same as that given in the previous paragraph.

5. <u>WDFs involving adaptors with more than two ports</u>

In certain types of WDFs one has to make use of adaptors with more than two ports. The question thus arises whether the present approach can be extended to such cases.

In principle this question can be answered in the affirmative. It is indeed always possible to introduce pairs of inverse multipliers as we have done in Section 2 and to make use of the freedom thus gained in order to introduce simplifications for the realization of the adaptors. Hence, one can take advantage of this possibility also in the case of adaptors with more than two ports.

In general, however, one cannot expect to arrive at as substantial a gain as in the case of two-port adaptors. The reason for this is that the number of entries of a matrix describing an adaptor increases with the square of the number of ports, while the number of degrees of freedom gained for an adaptor increases only linearly with the number of its ports.

It is thus clear that beyond the two-port adaptors the method appears to be most attractive in the case of three-port adaptors, which are also the ones that are most important in practice. We will not examine this in detail in this paper, but simply point out a few aspects.

We will have to expect that in the case of a three-port adaptor the resulting 6-pole block will be such that 2 multiply-accumulate steps will be necessary for each one of the 3 output signals (except for the output signal at a reflection-free port, which needs only one multiply-accumulate step). A difficulty arises in this case with respect to implementing a simple saturation characteristic, at least if the only possibility of doing it is to apply it after each multiply-accumulate step individually and if the three values to be added do not all have the same sign. A way of avoiding this difficulty is offered if none of the coefficients involved is larger than unity in modulus and if there exists a possibility to arrange the order of the computations in such

a way that the first accumulation step concerns two numbers of opposite sign. Even without the latter type of facility, however, overflow stability (as apposed to the more stringent forced-response stability) can be shown to remain guaranteed.

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Figure captions

Fig. 1 (a) A 1st-degree all-pass section
(b) A section derived from (a) by inserting pairs of inverse multipliers at appropriate locations
(c) Simplified representation of (b).

Fig. 2 (a) A second-degree all-pass section
(b) A section derived from (a) by inserting pairs of inverse multipliers at appropriate locations
(c) Simplified representation of (b).

Fig. 3 (a) An all-pass structure of degree n
(b) A structure derived from (a) by inserting, at appropriate locations, pairs of inverse multipliers and combining them (except for the two multipliers at the left) with the adaptor to which they are closest.

Fig. 4 (a) A lattice WDF with one input and one output terminal
(b) Corresponding structure obtained by realizing the all-pass functions S_1 and S_2 as explained in Section 2
(c) and (d) Equivalent structures derived from (b).

Fig. 5 (a) Full two-port lattice WDF
(b) Example of a structure derived from (a) by realizing the all-pass functions S_1 and S_2 as explained in Section 2.

Fig. 6 (a) A reference filter in form of a cascade of unit elements
(b) A corresponding WDF
(c) A structure derived from (b) by means of a method analogous to that described in Section 2.

Claims

1. Digital filter obtained by modifying a wave digital filter (WDF) characterized in that the original WDF is modified by inserting, into appropriately selected interconn cting leads, appropriately chosen pairs of (mutually) inverse multipliers (k_i; l/k_i...) and by incorporating, wherever possible, each such multiplier (k_i; l/k_i...) into the adaptor to which it is most adjacent, i.e., to which it is either directly adjacent or from which it is separated at most by a delay element wherein a structure resulting from an adaptor by incorporating into it the multipliers (k_i; l/k_i...) to which it is most adjacent being referred to hereafter as a modified adaptor.

2. Digital filter as claimed in claim 1 characterized in that the multipliers (k_i; l/k_i...) are chosen in such a way that the number of multiply-add operations required by the modified adaptors are as small as possible.

3. Digital filter as claimed in claim 2 characterized in that for any modified adaptor resulting, from a two-port adaptor the number of multiply-add operations required is exactly 2.

4. Digital filter as claimed in claim 3 characterized in that for any modified adaptor the values of the multiplier coefficients involved are both at most equal to unity.

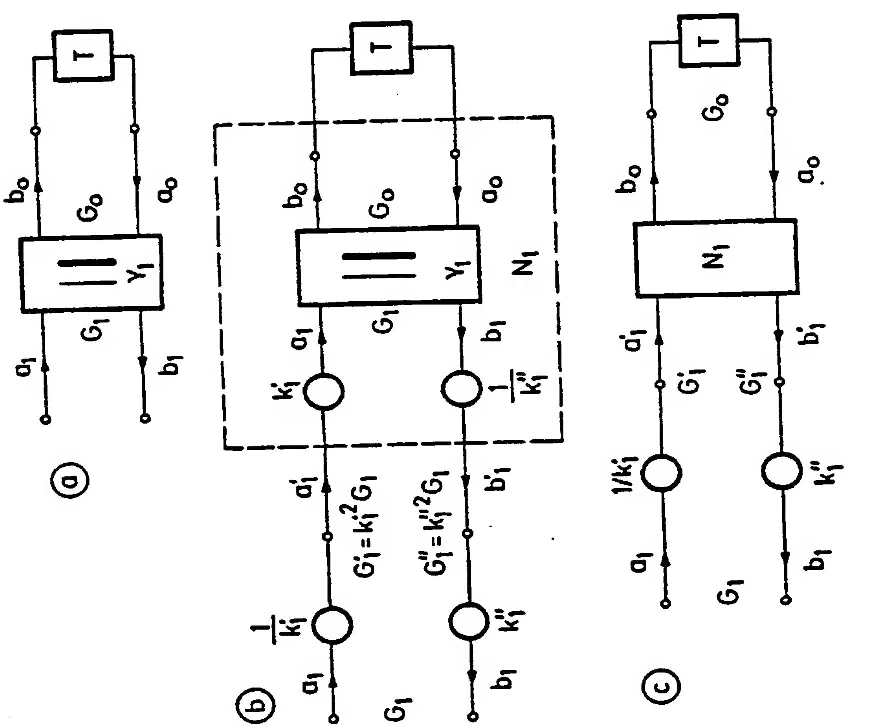
5. Digital filter as claimed in one of the claims 1 to 5 characterized in that the modified WDF is a lattice WDF.

6. Digital filter as claimed in one of the claims 1 to 5 characterized in that the modified WDF is such that it is obtained from a WDF whose adaptors are all two-port adaptors.

7. Digital filter as claimed in one of the preceding claims characterized in that the arithmetic operations in the modified adaptors are carried out in such a way that the output signals are detrermined according to a saturation characteristic.

8. Digital filter as claimed in one of the preceding claims characterized in that in the modified adaptors involved, the multipliers (k_i; l/k_i...) are quantized in such a way that these modified adaptors remain passive

Fig. 1
A. Fettweis



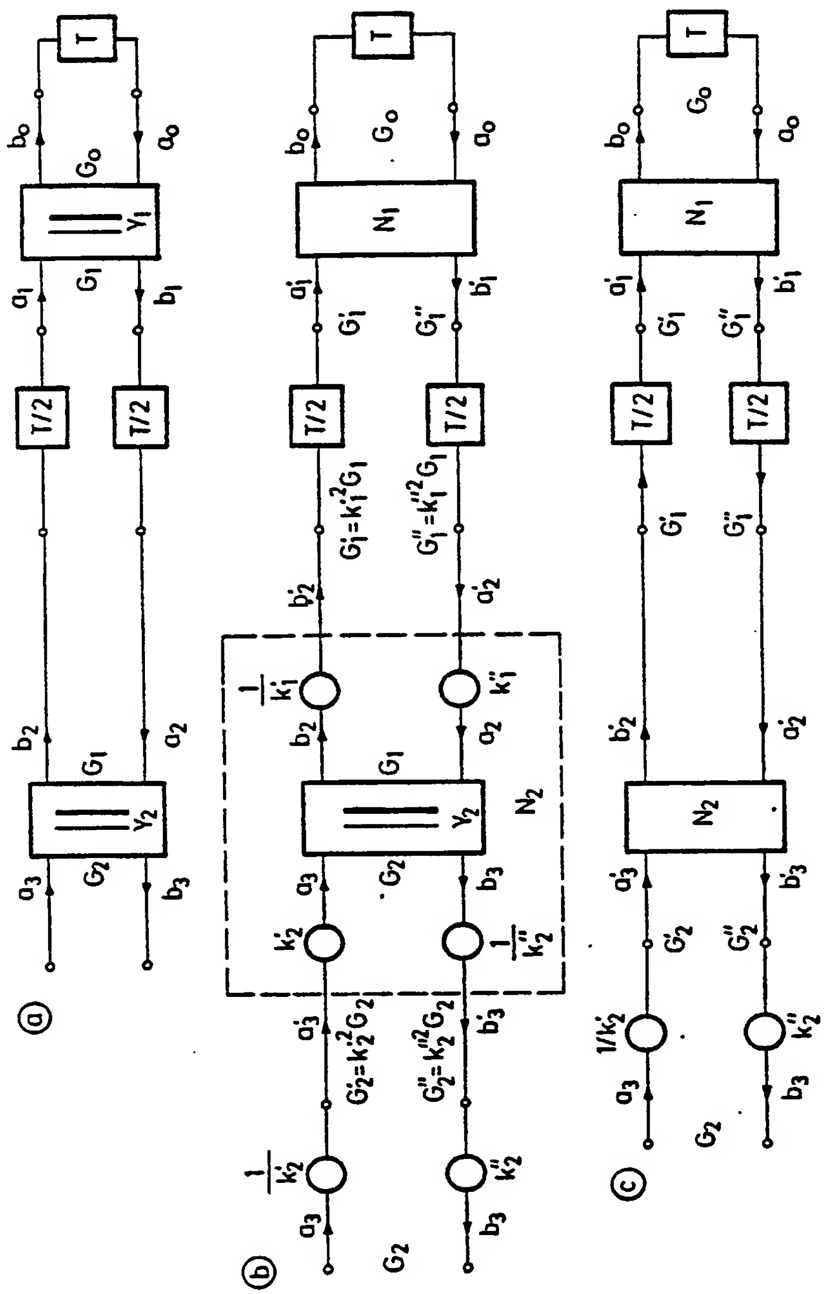


Fig 2
A. Fellweis

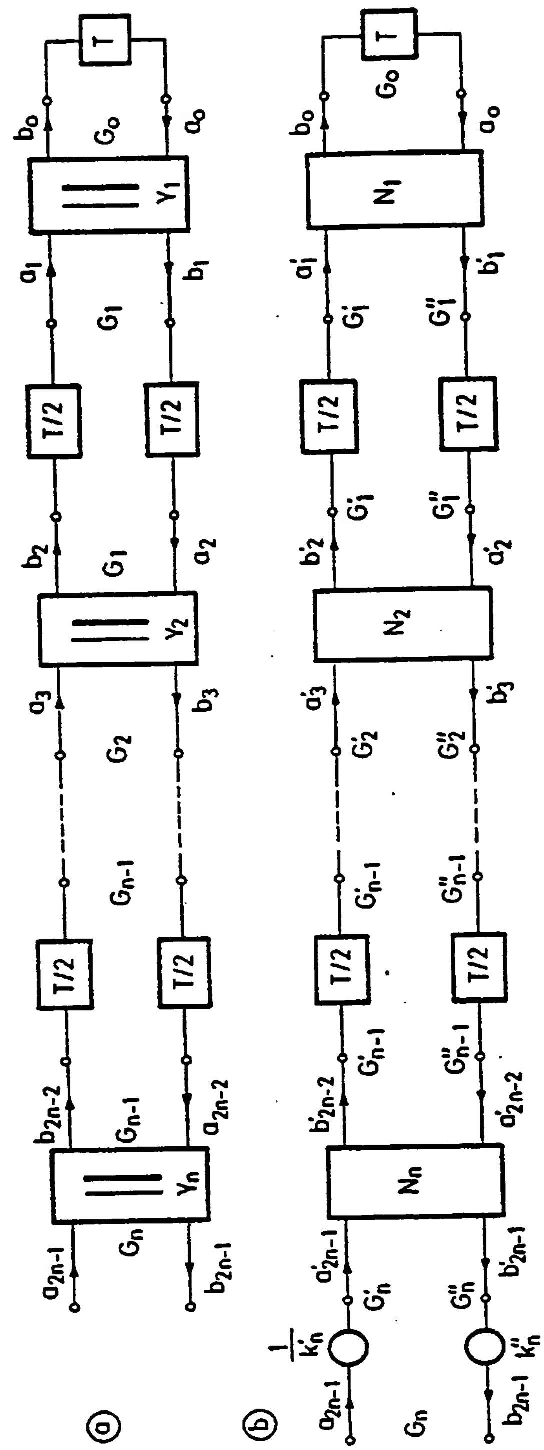


Fig 3
A. Fettweis

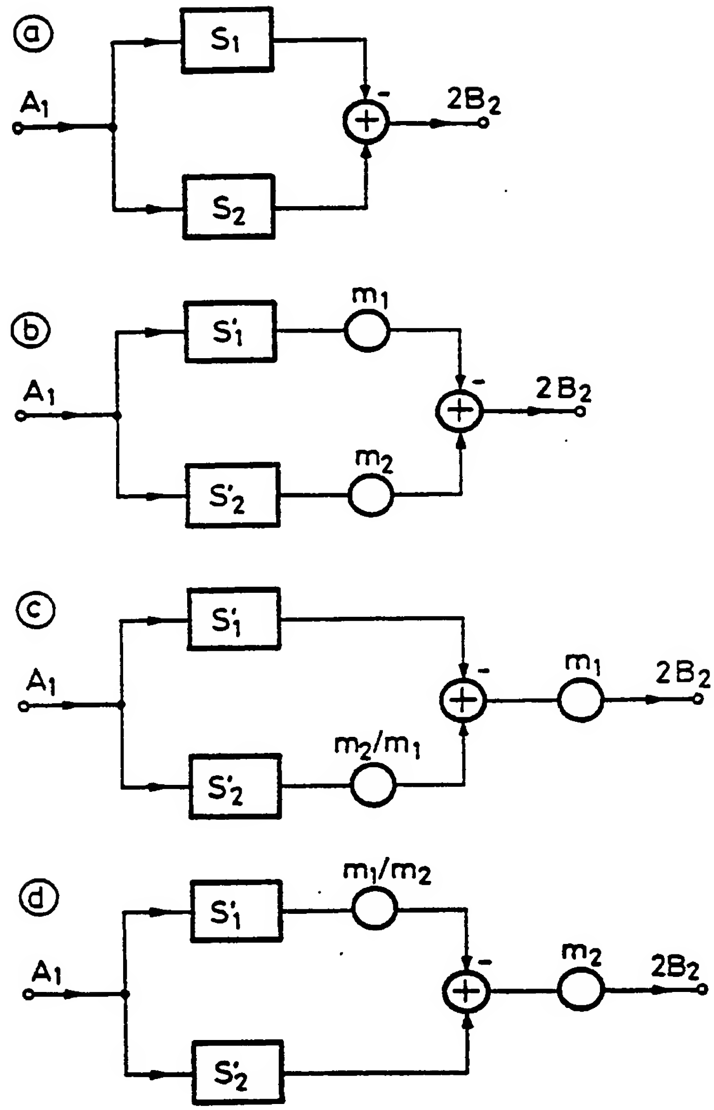


Fig. 4
A. Fettweis

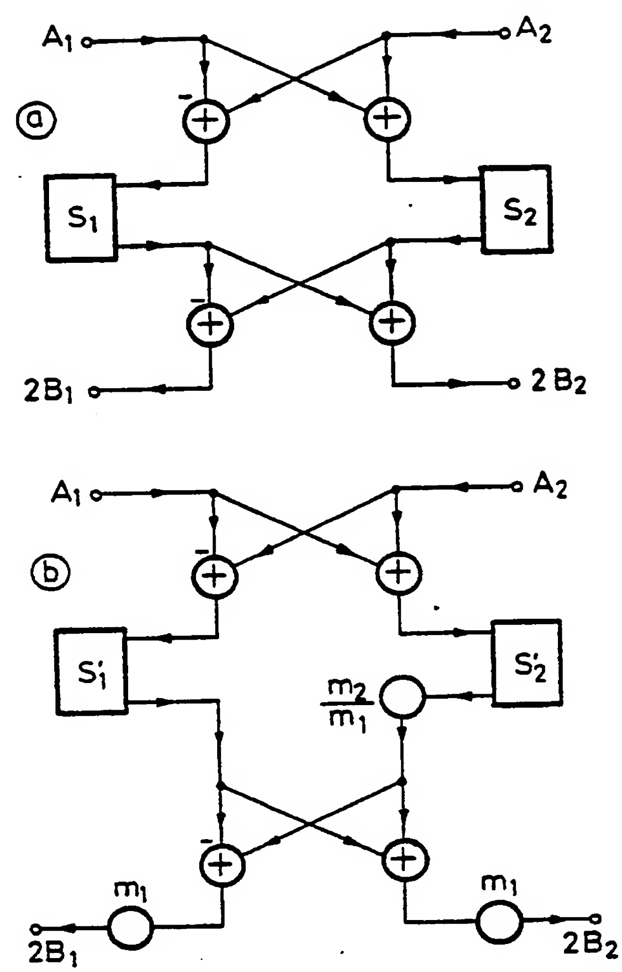


Fig. 5
A.Fettweis

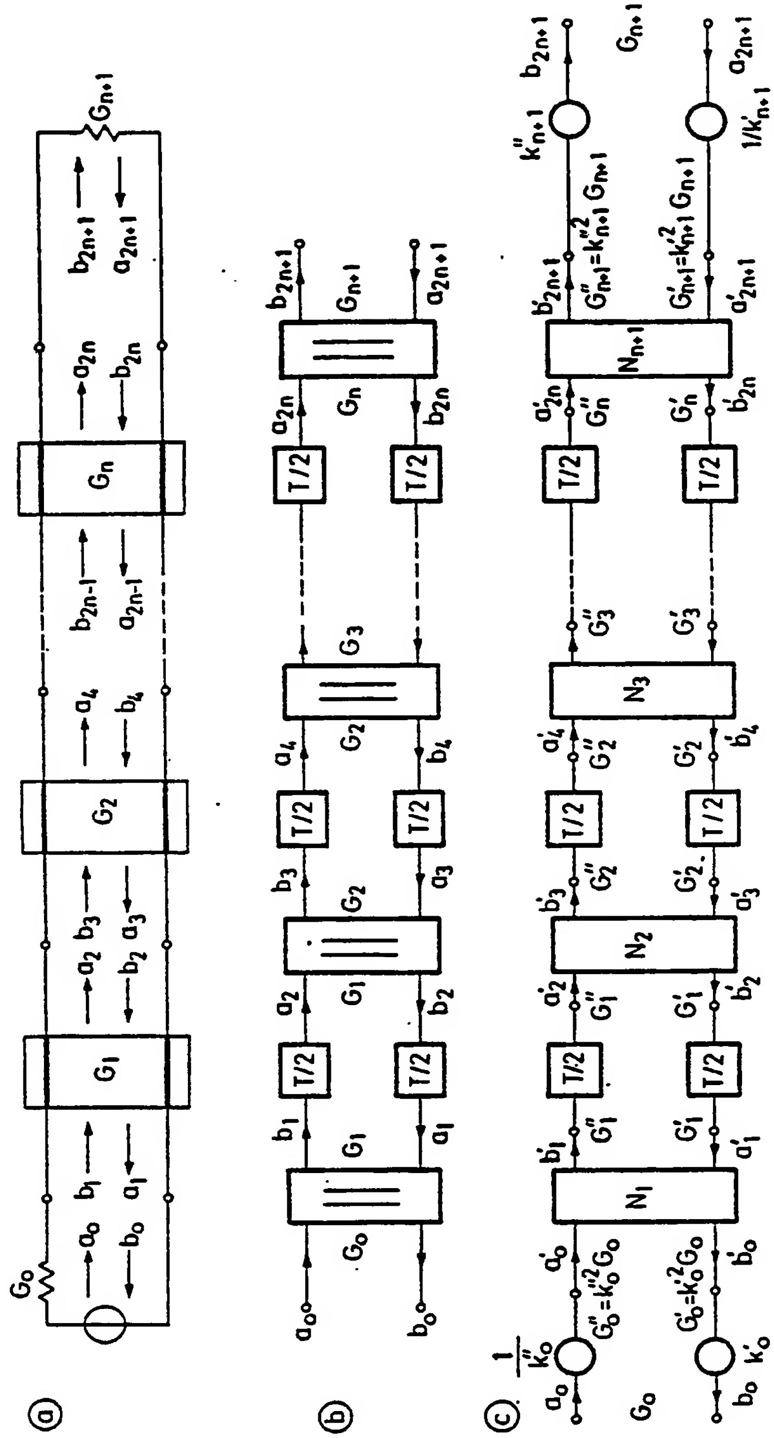


Fig 6
A.Fellweis

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EUROPEAN SEARCH REPORT

Application Number

EP 88 10 8525

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, vol. 1, 1973, pages 323-337, John Wiley & Sons, Ltd, Chichester, GB; A. FETTWEIS: "Reciprocity, inter-reciprocity, and transposition in wave digital filters" * Figure 4; pages 326-329: "General theorems on reciprocity, inter-reciprocity, and transposition" * -----	1	H 03 H 17/02
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
			H 03 H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25-01-1989	COPPIETERS C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
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